

# AXIe-0: Low-Cost Instrument Architecture

**Revision 1.0 DRAFT** 

January 28, 2022

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# **AXIe-0** Specification

# **Revision History**

This section is an overview of the revision history of the AXIe 1.0 specification.

| Revision Number | Date of Revision   | Revision Notes  |
|-----------------|--------------------|---|
| Preliminary     | September 11, 2014 | Initial Version, in slide format  |
| Revision 1.0    | January 28, 2022   | Changed name of spec to "Low-Cost Instrument Architecture".   |
|                 |                    | Formal textual specification.   |
|                 |                    | Added AXIe-0 Terms section  |
|                 |                    | Increased non-managed power capability from 50watts/slot to 200watts/slot.  |
|                 |                    | Added a Documentation section listing which device<br>capabilities and requirements are required to be<br>documented. This is to ensure compatibility between<br>chassis and modules. |
|                 |                    | Added CLK100 as required chassis feature.   |
|                 |                    | Eliminated nomenclature for AXIe-0 devices. No longer define or reference AXIe-0M or AXIe-1LC.  |
|                 |                    | Added P20 and P23 local bus as optional capability.   |
|                 |                    | Eliminated requirement to place AXIe compliance<br>label somewhere on module. This was to distinguish<br>AXIe-0 vs. AXIe-0M, but AXIe-0M no longer exists.                            |
|                 |                    | IPv6 operation is no longer required.   |
|                 |                    | No SCPI commands are required or recommended.   |
|                 |                    | No SCPI commands are required, so the requirement<br>to support 5025 ScpiRaw sockets has also been<br>removed.  |
|                 |                    |   |
|                 |                    |   |
|                 |                    |   |
|                 |                    |   |
|                 |                    |   |

Table 1-1. Architecture Specification Revisions

\_\_\_\_\_

# 1. Overview of the AXIe-0 Specification

# 1.1 Introduction

The AXIe-0 Modular LAN Instrument Specification expands the breadth of AXIe applications by introducing a platform suitable for low-cost instrumentation and switching. AXIe-0 retains the module size and board area of the current AXIe-1 Base Architecture, while delivering a cost-effective platform for vendors and users not needing the full capability of AXIe-1. This new LAN-based modular architecture enhances cost effectiveness and improves ease of implementation for vendors wanting to take advantage AXIe's space, power, and form factor for products that don't require a high-speed data infrastructure based on PCI Express. Typical products include electronic switching, loads, frequency converters, and a wide set of custom functionality designed by system integrators.

Of particular note is the upward compatibility model of AXIe-0 to AXIe-1. All AXIe-0 modules can be mixed and matched with AXIe-1 modules in an AXIe-1 chassis. Essentially, AXIe-0 is a subset of the AXIe-1 specification. It uses LAN for communication to each module, and all modules appear as LXI instruments to system software. Optional non-ASCII communication and use of the AXIe trigger bus enables high-speed switching and triggering, either with other AXIe-0 products, or with AXIe-1 modules in a combined system. Creative choosing of functionality within the AXIe-0 specification has allowed significant backplane, power, and management cost savings.



#### Figure 1-1: AXIe-0 is upwards compatible to AXIe-1.

Key applications enabled by AXIe-0 include large switching systems, RF Interface Units for aerospace and defense, and custom modules developed by system integrators and end users. With AXIe offering the same slot width and large board area as VXI, AXIe-0 is an ideal transition platform for VXI depot test applications, or any instrumentation requiring the large module size. AXIe-0 retains the same scalability of AXIe-1, ranging from small horizontal 2-slot chassis to large 14-slot systems.

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Figure 1-2: AXIe-0 chassis can come in different sizes, with 2 to 14 slots.

To achieve the low product and development goals of AXIe-0, several capabilities of AXIe-1 were eliminated, as shown in the following graphic:



Figure 1-3: An AXIe-0 module and backplane connectors

AXIe-0 retains the module size and board area of the current AXIe-1 Base Architecture, while delivering a costeffective platform for vendors and users not needing the full capability of AXIe-1. The module is 1.2 inches thick (30.48mm), 11.02 inches deep(280mm), and 12.7 inches (322.25mm) wide (or tall) depending on whether the module is horizontal or vertical. Like AXIe-1, a chassis may have anywhere from 2 slots to 14. Also, like AXIe-1, modules may be any integer number of slots wide.

The cost savings of AXIe-0 come from simplifying the power, cooling, management, and backplane. An entry level AXIe-0 chassis consists of a LAN GbE switch, a 12-lane 100MHz clock and AXIe trigger bus, and up to 200 watt/slot cooling and power. Eliminated are three backplane connectors along with the PCI Express fabric, the shelf (chassis) manager hardware and software, and the need for specialized controllers and interface cards. A single -48V power supply powers all modules. As in AXIe-1, Zone 3 is not accessed, though future standards may utilize this area for cable egress or customizable backplanes.

# How does AXIe-0 achieve its cost advantages?

# LAN-interface...

- reduces backplane layers
- simplifies chassis functions
- included on PCs already
- Single power supply voltage (-48V)
  - Avoids over-engineering of multiple rails
- Zone 2 connectors reduced from 5 to 2.
- Zone 3 connectors eliminated
- IPMI management eliminated
  - Up to 200 watts power and cooling w/o management

Figure 1-4: AXIe-0 cost advantages

#### AXIe-0 modules

AXIe-0 modules are exactly the same size as AXIe-1 modules. AXIe-0 modules are essentially simple, fast, LXI devices. As with LXI, SCPI (Standard Commands for Programmable Instruments) is not required. By eliminating the SCPI parser, command execution time can be significantly reduced. Conversely, SCPI may be implemented if desired by the instrument developer. The 12-lane trigger bus allows test sequences to execute quickly without any LAN commands.

By adopting LXI protocols, AXIe-0 devices will be discovered through standard LXI discovery software used by most of today's test system. This makes AXIe-0 easy to integrate into current test systems.

LAN brings several other benefits with it. A user can sequence power on the chassis or controller in any sequence, any number of times. There are no enumeration issues like those found with PCI Express. LAN is simultaneously ubiquitous and robust. Also, since the data fabric is gigabit ethernet, it is easy to add precision timing for data acquisition via IEEE-1588. This extends AXIe-0 to data acquisition.

![](_page_7_Figure_20.jpeg)

AXIe-0's large board size, LAN interface, and robust power and cooling allow it to meet many instrumentation applications. Key applications include:

- Large ATE switching systems. AXIe-0's deep module size enables efficient rack density.

- Second, but related, is the transition from VXI to AXIe for depot test systems used by the military and aerospace industry. The similar module size of AXIe to VXI eases this transition.

- A third application is custom instrumentation. Almost all large ATE systems have a need for custom electronics. These may include signal conditioning, load boards, or custom bus interfaces. These are typically designed by system integrators or end users. At low volumes, development costs swamp all other costs, so making these modules as easy as possible to design is important. The large board size, available power and cooling, and easy bus interface of AXIe-0 helps greatly in this regard.

- A fourth application includes a variety of products that can be best described as accessories, such as down-converters and up-converters, that can be implemented easily in this format. The upward compatibility of AXIe-0 modules into AXIe-1 systems allows many accessory products to be implemented in AXIe-0, but used in AXIe-1.

In general, any type of product that could be envisioned as an LXI rack mounted product can also be implemented in AXIe-0.

#### 1.2 Audience of Specification

This specification is primarily for the use of AXIe equipment manufacturers and system integrators who are implementing products and systems that conform to the requirements of this specification. The primary audience is assumed to have extensive knowledge of modular measurement hardware architectures, and access to the various referenced technical specifications. However, this specification should also prove useful to managers and anyone else involved in the selection of modular test system platforms and architectures.

#### 1.3 Organization of Specification

This specification consists of a system of numbered RULES, RECOMMENDATIONS, PERMISSIONS, and OBSERVATIONS, along with supporting text, tables, and figures.

**RULE**s outline the core requirements of the specification. They are characterized by the keyword "**SHALL**". Conformance to these rules provides the necessary level of compatibility to support the multi-vendor interoperability expected by system integrators and end users in the test and measurement industry. Products that conform to this specification must meet all of the requirements spelled out in the various rules.

**RECOMMENDATION**s provide additional guidance that will help AXIe equipment manufacturers improve their users' experiences with AXIe systems. They are characterized by the keyword "**SHOULD**". Following the recommendations should improve the functionality, flexibility, interoperability, and/or usability of AXIe products. Products are not required to implement the recommendations.

**PERMISSION**s explicitly highlight some of the flexibility of the AXIe specification. They are characterized by the keyword "**MAY**". The permissions generally clarify the range of design choices that are available to product and system designers at their discretion. They allow designers to trade off functionality, cost, and other factors in order to produce products that meet their users' expectations. Permissions are neutral and imply no preference as to their implementation.

**OBSERVATION**s explicitly highlight some of the important nuances of the specification. They help the readers to fully understand some of the implications of the specification's requirements and/or the rationale behind particular requirements. They generally provide valuable design guidance.

All rules, recommendations, permissions, and observations must be considered in the context of the surrounding text, tables, and figures. Rules may explicitly or implicitly incorporate information from the text, tables, and figures.

AXIe-0 Revision 1.0, January 28, 2022

Although the authors of this specification have gone to significant effort to insure that all of the necessary requirements are spelled out in the rules, it is possible that some important requirements appear only in the specification's free text. Conservative design practice dictates that such embedded requirements be treated as rules.

The AXIe-0 specification, like the AXIe-1 specification, is based on the AdvancedTCA<sup>®</sup> specification. Successful implementation of AXIe-0 products and systems requires in-depth knowledge of this AXIe-0 specification, the AXIe-1 specification, the AdvancedTCA<sup>®</sup> specification, and the LXI Device Specification.

### 1.4 Architecture Overview

The AXIe-0 architecture consists of hardware and software requirements that support the smooth multi-vendor integration of AXIe-0 modules and chassis into powerful test systems. The requirements also enable the integration of AXIe-0 modules into AXIe-1 chassis and systems. The AXIe-0 specification fits into the AXIe hierarchy as shown in the diagram below. The AXIe Consortium also supports the high speed ODI (Optical Data Interface) specification. The ODI specification is not form factor dependent. AXIe-0 instruments, like any other, may implement ODI interfaces.

| AXIe-3.n | Semiconductor<br><u>Test</u> AXIe-3.1<br>• Zone 3 signals:<br>• Trigger/Sync<br>• DUT I/O | Other future<br>Apps AXIe-3.n<br>• Other Zone 3 may<br>be standardized in<br>future |  | <ul> <li>AXIe-3.n specifications define Zone<br/>3 capabilities for specific markets</li> <li>A vendor may add a custom Zone 3<br/>backplane that is not a AXIe-3.n<br/>specification</li> </ul> |
|----------|---|---|--|--|
| AXIe-3   | AXle Zone 3 Mech     By-slot customization  | anical<br>on of Zone 3 backplane  |  | • AXIe-3 specifies mounting positions to add multiple Zone 3 backplanes  |
| AXIe-2   | AXIe Software Spe     Discovery, Configur   | ecification<br>ation, and Control   |  | <ul> <li>AXIe-2 utilizes PXI for its module<br/>and chassis software requirements</li> </ul>   |
| AXIe-1   | AXle Base Architecture     ATCA + Triggers + Timing + Local Bus                           |   |  | <ul> <li>AXIe-1 is the core specification for<br/>AXIe, and dominates the market</li> </ul>  |
| AXIe-0   | Low-Cost Instrum     LAN-based, simplif   | ent Architecture<br>ied system management   |  | <ul> <li>AXIe-0 is a low-cost subset of AXIe-<br/>1 specification for LAN-based<br/>instrumentation.</li> </ul>  |
| AXIe-CR  | Compliance Requi     Compliance and Tra   | i <b>rements</b><br>ademark usage   |  | <ul> <li>AXIe-CR lists requirements to claim<br/>conformance and use AXIe logo</li> </ul>  |
| ATCA     | AdvancedTCA PIC     LAN + PCIe + Syste  | CMG3.0, PICMG3.4<br>em management   |  | • ATCA is the underlying specification for all AXIe specifications   |

![](_page_9_Figure_5.jpeg)

#### 1.5 Terminology

AXIe terminology is modeled largely on language familiar to manufacturers, system integrators, and end users in the test and measurement industry. In many cases this is different from the telecom-derived terminology used in the AdvancedTCA<sup>®</sup> specification.

### 1.5.1 AXIe-0 Terms

Here are the definitions of some of the more common AXIe terms:

- *Chassis* This is the primary AXIe-0 infrastructure component that hosts AXIe-0 modules. A typical AXIe-0 chassis includes a backplane, subrack, power supply(ies), fan tray(s), and sheet metal enclosure. It may include rack mounting provisions. Unlike AXIe-1, an AXIe-0 will not include a shelf manager. A chassis may also include an *embedded system module*. (See *Integrated Chassis*.)
- *Integrated Chassis* An AXIe chassis that has built-in system module functionality in lieu of an AXIe-standard system slot.
- *Module* A PC assembly, face plate, and enclosure that plugs into an AXIe slot. Equivalent to an AdvancedTCA<sup>®</sup> *front board*.
- *System Module* An AXIe module that includes LAN switches, system timing and trigger resources, and/or other central resources. A system module installs in a chassis system slot. An AXIe system module is comparable to an AdvancedTCA<sup>®</sup> *hub board*.
- Embedded System Module System module functionality that is embedded in an integrated chassis.
- System Slot An AXIe slot that supports a system module. It is always logical slot 1. It is comparable to an AdvancedTCA<sup>®</sup> hub slot.
- *IPMI* Intelligent Platform Management Interface is a standardized interface in ATCA and AXIe for system management of the chassis and modules. It is not required for AXIe-0.
- Instrument Module Any AXIe module that is not a system module.
- *Base Fabric* The electrical interconnections on the backplane that transport GbE LAN to each slot.
- *AXIe Timing Interface* A collection of star-topology signal pairs that carry AXIe timing signals between the *system slot* and the *instrument slots*. The timing signals are CLK100, SYNC, STRIG, and FCLK.
- *AXIe Trigger Bus* A set of 12 MLVDS signal pairs, TRIG(0:11), that are bused across all the slots of an AXIe backplane.
- *CLK100* A set of 100 MHz LVDS signal pairs that is sourced by the *system module*, buffered on the AXIe backplane, and transmitted to all *instrument modules* in a star topology.
- *SYNC* A set of LVDS trigger/synchronization signal pairs that is sourced by the *system module*, buffered on the AXIe backplane, and transmitted to all *instrument modules* in a star topology.
- *STRIG* (*Star Trigger*) A set of bi-directional LVDS signal pairs that directly connects the *system slot* to all of the *instrument slots* in a star topology.
- *FCLK (Fabric Clock)* A set of 100 MHz HCSL signal pairs that is sourced by the *system module*, buffered on the AXIe backplane, and transmitted to all *instrument modules* in a star topology. This fabric clock is the PCI Express<sup>®</sup> reference clock for all PCI Express<sup>®</sup> ports on the fabric channels connected to the system slot.
- *LXI* LAN eXtensions for Instrumentation is a standard for LAN equipped instrumentation. It is sponsored by the LXI Consortium, and the standards may be found on the website here: <u>https://www.lxistandard.org</u>
- *IVI* Interchangeable Virtual Instruments is a set of standards managed by the IVI Foundation that addresses programmable instruments. The website may be found here: <u>https://www.ivifoundation.org</u>
- *SCPI* Standard Commands for Programmable Instruments is a standard for instrument command languages. The specification may be found here: <u>https://www.ivifoundation.org/docs/scpi-99.pdf</u>

# 2. AXIe-0 Chassis and Modules

AXIe-0 modules and chassis are essentially a subset of AXIe-1 modules and chassis. In almost all cases the current AXIe-1 specification has the detailed requirements for any particular AXIe-0 functionality.

### 2.1 General Mechanical Requirements

AXIe-0 modules and chassis are mechanically the same as AXIe-1 modules.

RULE 2.1: AXIe-0 products SHALL conform to all mechanical requirements of the AXIe-1 specification.

## 2.2 AXIe-0 Chassis and System Modules

AXIe-0 modules and chassis are mechanically the same as AXIe-1 modules.

#### RULE 2.2: AXIe-0 products SHALL conform to all mechanical requirements of the AXIe-1 specification.

An AXIe-0 chassis may be configured to have an explicit slot for an AXIe System Module (ESM), or it may be configured to include the functionality of an ASM built into the chassis as an Embedded System Module (ESM)

**RULE 2.3:** An AXIe-0 chassis SHALL be configured with an explicit slot for an AXIe System Module or configured to include embedded AXIe System Module functionality within the chassis.

PERMISSION 2.1: An AXIe-0 chassis MAY include an explicit slot for an AXIe System Module.

**PERMISSION 2.2:** An AXIe-0 chassis MAY include embedded AXIe System Module functionality within the chassis, without an explicit slot.

#### 2.2.1 AXIe-0 System Module

The AXIe-0 System Module functionality, whether an explicit slot or embedded, includes a LAN switch that routes to each non-system slot and a 100MHz Clock defined by AXIe CLK 100 that is also routed to each non-system slot. The LAN routing is defined within the Base Fabric specifications of AXIe-1.

RULE 2.4: An AXIe-0 chassis with an explicit ASM slot SHALL route the Base Fabric to each non-system slot.

RULE 2.5: An AXIe-0 chassis with embedded system module functionality SHALL route a GBE port to the Base Fabric of each non-system slot.

RULE 2.6: An AXIe-0 chassis with an explicit ASM slot SHALL route CLK100 to each non-system slot.

RULE 2.7: An AXIe-0 chassis with embedded system module functionality SHALL generate and route a CLK100 signal to each non-system slot.

The AXIe System Module function, whether explicit or embedded, may include additional functionality beyond the required functionality of LAN and CLK100.

## 2.3 AXIe-0 Chassis and Module Size

AXIe-0 modules and slots are the same size as AXIe-1 modules and slots.

PERMISSION 2.3: An AXIe-0 chassis may be any number of slots and slot orientation.

PERMISSION 2.4: An AXIe-0 module may be any integer number of slots wide.

**RULE 2.8:** The Geographical Address of a multi-slot module SHALL be determined by the lowest logical slot number.

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**OBSERVATION 2.1:** For a multi-slot module, the Geographical Address is typically the left-most slot of that module when placed in a vertical orientation.

### 2.4 AXIe-0 Power and Cooling

AXIe-0 offers non-managed power and cooling up to 200 watts/slot. Because an AXIe-0 chassis is unmanaged, it is necessary for each module to state its power and cooling requirement, and each chassis to state its power and cooling capability. This allows a system integrator to choose compatible AXIe-0 modules and chassis.

RULE 2.9: An AXIe-0 chassis SHALL specify its total and per-slot power and cooling capacity.

RULE 2.10: An AXIe-0 module SHALL specify its total and per-slot power and cooling requirements.

**OBSERVATION 2.2:** For a single-slot AXIe-0 module, the total and per-slot power and cooling requirements are the same.

PERMISSION 2.5: A single-slot AXIe-0 module is only required to state its total power and cooling requirement.

**OBSERVATION 2.3:** The power requirements and cooling requirements of an AXIe module are often the same. They may differ when additional power may be dissipated within a module through a load function or when power supplied by the chassis may be dissipated external to the module.

PERMISSION 2.6: An AXIe-0 module that does not have a significant difference between its power requirement and cooling requirement is only required to state its total power requirement.

## 2.5 AXIe-0 Backplane and Module Connectors

An AXIe-0 chassis is required to have three connectors: The Zone 1 connector and Zone 2 connectors P20 and P23. All other connectors are optional. Zone 3 connectors are not allowed in AXIe-0 or AXIe-1, but may be addressed in future standards.

![](_page_12_Figure_11.jpeg)

Figure 2-1: AXIe chassis showing the three connector zones. AXIe-0 Revision 1.0, January 28, 2022

#### 2.5.1 Zone 1 Connector

AXIe-0 chassis must include the Zone 1 connector. This connector supplies -48V power and Slot ID used for geographical addressing.

#### RULE 2.11: An AXIe-0 chassis SHALL include a Zone 1 connector.

#### RULE 2.12: An AXIe-0 mainframe SHALL include Slot ID coded into the Zone 1 connector.

Nearly every AXIe-0 module will include a Zone 1 connector. The exception to this is an unpowered module, such as a load.

#### PERMISSION 2.7: An AXIe-0 MAY include a Zone 1 module.

#### PERMISSION 2.8: An AXIe-0 MAY include detect and report their Slot ID.

#### 2.5.2 Zone 2 Connectors

AXIe-0 chassis must include Zone 2 connectors P20 and P23.

The LAN base fabric is routed to P23 of each slot, exactly as with AXIe-1.

| D   | Terterform        | Instrument Slot (Logical Slots 2-14) J23/P23 Connector Pairs |                   |                   |                   |          |          |          |          |
|-----|-------------------|--|-------------------|-------------------|-------------------|----------|----------|----------|----------|
| KOW | Interface         | a  | b                 | C                 | d                 | e        | f        | g        | h        |
| 1   | Fabric            | Tx2[2]+  | Tx2[2]-           | Rx2[2]+           | Rx2[2]-           | Tx3[2]+  | Tx3[2]-  | Rx3[2]+  | Rx3[2]-  |
| 2   | Channel 2         | Tx0[2]+  | Tx0[2]-           | Rx0[2]+           | Rx0[2]-           | Tx1[2]+  | Tx1[2]-  | Rx1[2]+  | Rx1[2]-  |
| 3   | Fabric            | Tx2[1]+  | Tx2[1]-           | Rx2[1]+           | Rx2[1]-           | Tx3[1]+  | Tx3[1]-  | Rx3[1]+  | Rx3[1]-  |
| 4   | Channel 1         | Tx0[1]+  | Tx0[1]-           | Rx0[1]+           | Rx0[1]-           | Tx1[1]+  | Tx1[1]-  | Rx1[1]+  | Rx1[1]-  |
| 5   | Base<br>Channel 1 | BI_DA1+<br>(TX1+)  | BI_DA1-<br>(TX1-) | BI_DB1+<br>(RX1+) | BI_DB1-<br>(RX1-) | BI_DC1+  | BI_DC1-  | BI_DD1+  | BI_DD1-  |
| 6   | Local Bus         | LBL[8]+  | LBL[8]-           | LBL[9]+           | LBL[9]-           | LBR[8]+  | LBR[8]-  | LBR[9]+  | LBR[9]-  |
| 7   | Local Bus         | LBL[10]+   | LBL[10]-          | LBL[11]+          | LBL[11]-          | LBR[10]+ | LBR[10]- | LBR[11]+ | LBR[11]- |
| 8   | Local Bus         | LBL[12]+   | LBL[12]-          | LBL[13]+          | LBL[13]-          | LBR[12]+ | LBR[12]- | LBR[13]+ | LBR[13]- |
| 9   | Local Bus         | LBL[14]+   | LBL[14]-          | LBL[15]+          | LBL[15]-          | LBR[14]+ | LBR[14]- | LBR[15]+ | LBR[15]- |
| 10  | Local Bus         | LBL[16]+   | LBL[16]-          | LBL[17]+          | LBL[17]-          | LBR[16]+ | LBR[16]- | LBR[17]+ | LBR[17]- |

Figure 2-2: Zone 2 P23 Connector pinout, showing location of Base Fabric

RULE 2.13: An AXIe-0 chassis SHALL route the Base Fabric Channel 1 to P23 of each slot.

**OBSERVATION 2.4:** The Base Fabric Channel 1 is the only required signal or functionality on P23. **PERMISSION 2.9:** An AXIe-0 chassis MAY route other signals on P23 in accordance with AXIe-1.

Zone 2 P20 includes 12 LVDS Trigger lines denoted as AXIe TRIG [0:11] and CLK100 signals. It may also include FCLK, SYNC, and STRIG signals. The 12 AXIe trigger bus, TRIG[0:11] pairs are bused across all 14 slots, including the system module, connecting to corresponding pins on each slot.

| D   | <b>T</b> ( 6 | Instrument Slot (Logical Slot 2-14) J20/P20 Connector Pairs |           |          |          |          |          |           |           |  |
|-----|--------------|---|-----------|----------|----------|----------|----------|-----------|-----------|--|
| Row | Interface    | a   | b         | C        | cd       |          | ef       |           | gh        |  |
| 1   | Trigger      | TRIG[0]+  | TRIG[0]-  | TRIG[1]+ | TRIG[1]- | TRIG[2]+ | TRIG[2]- | TRIG[3]+  | TRIG[3]-  |  |
| 2   | Trigger      | TRIG[4]+  | TRIG[4]-  | TRIG[5]+ | TRIG[5]- | TRIG[6]+ | TRIG[6]- | FCLK+     | FCLK-     |  |
| 3   | Trigger      | TRIG[7]+  | TRIG[7]-  | TRIG[8]+ | TRIG[8]- | TRIG[9]+ | TRIG[9]- | TRIG[10]+ | TRIG[10]- |  |
| 4   | Timing       | TRIG[11]+   | TRIG[11]- | STRIG+   | STRIG-   | SYNC100+ | SYNC100- | CLK100+   | CLK100-   |  |
| 5   | Local Bus    | LBL[0]+   | LBL[0]-   | LBL[1]+  | LBL[1]-  | LBR[0]+  | LBR[0]-  | LBR[1]+   | LBR[1]-   |  |
| 6   | Local Bus    | LBL[2]+   | LBL[2]-   | LBL[3]+  | LBL[3]-  | LBR[2]+  | LBR[2]-  | LBR[3]+   | LBR[3]-   |  |
| 7   | Local Bus    | LBL[4]+   | LBL[4]-   | LBL[5]+  | LBL[5]-  | LBR[4]+  | LBR[4]-  | LBR[5]+   | LBR[5]-   |  |
| 8   | Local Bus    | LBL[6]+   | LBL[6]-   | LBL[7]+  | LBL[7]-  | LBR[6]+  | LBR[6]-  | LBR[7]+   | LBR[7]-   |  |
| 9   | Local Bus    | LBL[38]+  | LBL[38]-  | LBL[39]+ | LBL[39]- | LBR[38]+ | LBR[38]- | LBR[39]+  | LBR[39]-  |  |
| 10  | Local Bus    | LBL[40]+  | LBL[40]-  | LBL[41]+ | LBL[41]- | LBR[40]+ | LBR[40]- | LBR[41]+  | LBR[41]-  |  |

Figure 2-3: Zone 2 P20 Connector pinout, showing location of trigger lines and CLK100.

![](_page_14_Figure_3.jpeg)

Figure 2-4: Zone 2 P20 CLK100 Buffering and Routing

![](_page_15_Figure_0.jpeg)

Figure 2-5: Zone 2 P20 CLK100 Routing

RULE 2.14: An AXIe-0 chassis SHALL route CLK100 and TRIG[0-11] onto P20 as described in AXIe-1.

**OBSERVATION 2.5:** CLK100 and TRIG[0-11] are the only required signals on P20.

PERMISSION 2.10: An AXIe-0 chassis MAY route other signals on P20 in accordance with AXIe-1.

PERMISSION 2.11: An AXIe-0 chassis or system module MAY allow CLK100 to be driven by an external connector.

PERMISSION 2.12: An AXIe-0 chassis or system module MAY route the TRIG lines to external connectors.

PERMISSION 2.13: An AXIe-0 chassis or system module MAY generate trigger signals on AXIe TRIG lines.

PERMISSION 2.14: An AXIe-0 chassis or system module MAY report the state of each trigger line.

PERMISSION 2.15: An AXIe-0 module MAY access the TRIG lines.

RULE 2.15: If an AXIe-0 module, other than a PXI Carrier, access any TRIG line, it SHALL access all twelve [0-11].

**RULE 2.16:** If an AXIe-0 module is a PXI Carrier, it SHALL map the PXI trigger lines to the similarly numbered eight AXIe TRIG lines [0-7].

**OBSERVATION 2.6:** The two rules above are designed to reduce oversubscribing to TRIG lines by making all TRIG lines accessible. The exception for PXI Carriers recognizes that PXI modules have a maximum of eight trigger lines. By mapping PXI and AXIe trigger lines, this guarantees the PXI instrument drivers will work the same as in a PXI system.

The inclusion of P20 and P23 allows the use of AXIe's local bus. The AXIe local bus provides short differential signal pairs between adjacent AXIe slots, excluding the system slot. In AXIe-1, there are 18 required local bus pairs in each slot-to-slot segment. Backplanes may optionally provide local bus expansion to 42 or 62 pairs. AXIe-1 local bus topology is shown below.

![](_page_16_Figure_1.jpeg)

Figure 2-6: AXIe-1 local bus topology

In AXIe-0 there are 22 local bus pairs between the P20 and P23 connectors. These can be used by AXIe-0 device manufacturers to facilitate communication between modules without using LAN protocols.

PERMISSION 2.16: An AXIe-0 module MAY access any or all local bus pairs on the J20 and J23 connectors.

RULE 2.17: If an AXIe-0 module accesses any local bus pair, it SHALL document that it uses the local bus.

PERMISSION 2.17: An AXIe-0 chassis MAY route local bus pairs between adjacent slots.

**RULE 2.18:** If an AXIe-0 chassis routes any local bus pair between slots, it SHALL route all 22 local bus pairs on the P20 and P23 connectors to the adjacent slots and document that it offers the local bus.

The rules above allow any AXIe-0 module that access the local bus to operate within any AXIe-0 chassis that offers the local bus.

#### 2.5.3 Zone 3 Connector

AXIe-0 systems do not use Zone 3 resources. However, the AXIe 3.n extension specifications are allowed to incorporate Zone 3 features appropriate for their respective marketplaces. The dimensions of AXIe 3.n Zone 3 midplane connectors are restricted to prevent interference with AXIe-0 and AXIe-1 modules. Like AXIe-1 chassis, AXIe-0 chassis are designed to mechanically accept AdvancedTCA<sup>®</sup> and AXIe 3.n modules that have Zone 3 connectors. This allows AXIe-0 and AXIe-1 modules to be inserted into AXIe 3.n chassis. This also allows for future standards to be added to AXIe-0 for accessing the Zone 3 region. One possible future application is cable ingress and egress.

#### RULE 2.19: AXIe-0 chassis SHALL NOT have any Zone 3 connectors.

#### RULE 2.20: AXIe-0 modules SHALL NOT have any Zone 3 connectors.

#### 2.5.4 Cabling access and Rear Transition Modules

The AXIe 1.0 Architecture does not include the use of Rear Transition Modules or module connections to Zone 3 connectors. Section 2.3 of the AdvancedTCA<sup>®</sup> specification, "RTM assembly" is not applicable to AXIe 1.0.

#### RULE 2.21: AXIe 1.0 modules SHALL NOT have any Zone 3 connectors.

#### 2.6 IPMI Requirements

There are no IPMI requirements for either, AXIe-0 chassis or modules. Management is not required for modules requiring less than 200 watts per slot.

# 3. AXIe-0 LAN Protocols

The AXIe-0 LAN protocols are at the communications heart of the AXIe-0 standard. Essentially, LAN is distributed from a host controller, through the explicit or embedded system module, and then via the base fabric to each slot. Each module acts as an independent LAN instrument. Lan Extensions for Instrumentation, or LXI, protocols are used between the controller and the modular instruments. AXIe-0 devices comply with a subset of the LXI base specification to facilitate discovery, setup, and communication. The diagram below shows a simple diagram of LAN connectivity between the host controller, the AXIe-0 chassis, and the modules. The figure shows a chassis with an embedded system module, but a system with an explicit system module would operate the same, but the LAN switch would be on the AXIe system module.

# LAN Protocols – Chassis Diagram

![](_page_18_Figure_3.jpeg)

Figure 3-1: Chassis LAN Functionality

In general, chassis intelligence is low or non-existent, while the instrument functionality is embedded in the modules and drivers. An explicit or embedded system module supports one or more external LAN connections to an external controller, and routes these to a switch that routes LAN to each slot.

A chassis or system module may have its own intelligence and associated IP address. If so, that intelligence is called a *chassis instrument*. This intelligence is typically located on the system module, whether an explicit or embedded system module.

The remainder of this document refers to a chassis instrument but could equally refer to the system module.

### 3.1 Chassis Requirements

**RULE 3.1:** An AXIe-0 chassis SHALL include a LAN switch to each slot, whether through an explicit system module or an embedded system module.

PERMISSION 3.1: An AXIe-0 chassis MAY include a chassis instrument.

RULE 3.2: An AXIe-0 chassis LAN switch SHALL support Auto-MDIX at its external connection.

**RECOMMENDATION 3.1:** A chassis instrument SHOULD support an ICMP ping responder, which is disableable.

**RECOMMENDATION 3.2:** A chassis instrument SHOULD be able to report on the state of any TRIG line, and generate triggers on TRIG lines.

**OBSERVATION 3.1:** The chassis instrument is an ideal location to implement optional IEEE 1588 once for an entire chassis with modules.

**OBSERVATION 3.2:** In general, any LAN protocol requirement for AXIe-0 modules is also a requirement for a chassis instrument if one exists.

### 3.2 LAN/LXI Functionality

AXIe-0 makes use of the LXI specifications developed by the LXI Consortium, and can be found at: <u>https://www.lxistandard.org/Specifications/Specifications.aspx</u>

The LXI specifications consist of:

- (1) a core specification, LXI Device Specification 2016, to which all LXI Devices must conform; and
- (2) a set of optional Extended Features, to which vendors may choose to conform. Vendors are required to declare to which Extended Functions (if any) they conform.

This section will be organized to reflect the organization of LXI Device Specification 2016, which will be referred to as simply the LXI Specification. Specifically, the third digit of this AXIe-0 section will reflect the chapter number of the LXI Specification. Thus, we have the following sections:

3.2.1 LXI Overview
3.2.2 LXI Physical Specifications
3.2.3 LXI Device Synchronization and Events
3.2.4 Module-to-Module Data Communication of LXI Event Messages
3.2.5 LXI Device Wired Trigger Bus
3.2.6 LXI Programmatic Interface (Drivers)
3.2.7 LAN Specifications
3.2.8 IPV4 LAN Configuration
3.2.9 Web Interface
3.2.10 LAN Discovery and Identification
3.2.11 Documentation

Any Extended Functions relevant to AXIe-0 will be documented in section 3.3 LAN/LXI Extended Functions

#### 3.2.1 LXI Overview

The equivalent LXI section is largely an overview of the LXI specification structure. This LXI section includes required declarations of LXI Device Specification compliance, both the LXI Version, and the LXI Extended Functions. AXIe-0 waives these requirements. Furthermore, the LXI Trademark is not required on any AXIe-0 devices. Technically, by waiving these requirements, AXIe-0 modules may not be fully compliant LXI devices. If a

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developer wishes to use the LXI logo on a non-compliant product they must first get permission from the LXI Consortium.

# **PERMISSION 3.2:** An AXIe-0 device is not required a declare that it is LXI conformant, nor must it supply a list of LXI Extended Functions.

# **PERMISSION 3.3:** An AXIe-0 device is not required to place an LXI Trademark anywhere on the physical device or related software.

#### 3.2.2 LAN/LXI Physical Specifications

This part of the AXIe-0 and LXI specifications deals with faceplate or front panel indicators, labels, and required buttons.

#### 3.2.2.1 Faceplate/Front Panel Indicators

LXI requires Power and LAN Status indicators on the front panel of an LXI device. LXI recommends, but does not specify, specific LED colors and illumination for indicating power and LAN status. This approach has been migrated to AXIe modules, with indicators required on the module to indicate power and LAN status.

**RULE 3.3:** An AXIe-0 module that requires power from the chassis SHALL indicate the state of the power through one or more indicators on the faceplate.

# **RULE 3.4:** An AXIe-0 module that utilizes LAN supplied by the chassis SHALL indicate the status of the LAN through one or more indicators on the faceplate.

LXI allows IEEE 1588 operation via the LAN connection. AXIe-0 also allows IEEE 1588 operation.

# **RULE 3.5:** If an AXIe-0 module employs IEEE-1588 operation via the LAN connection, THEN the module SHALL indicate the IEEE-1588 Clock Status through one or more indicators on the faceplate.

The above rules give considerable latitude to the design and placement of indicators on an AXIe-0 module. This mirrors the flexibility of LXI.

**OBSERVATION 3.3:** Any reasonable method of displaying the Power and LAN Status on the module faceplate will be accepted, including the use of alpha-numeric, non-LED, and graphical displays.

# **RULE 3.6:** An AXIe-0 module that utilizes LAN SHALL make use of the LAN Status Indicators to inform the user of a LAN fault or error caused by failures articulated in RULE 8.10 of the LXI Specification titled Provide an Error Indicator for LAN Configuration Faults.

The above rules address indicator requirements for modules. AXIe-0 chassis are also required to indicate their power status.

#### RULE 3.7: A Power Indicator SHALL be provided on an AXIe-0 chassis.

AXIe-0 does not specify the location or the operation of the Power Indicator.

Though the above rules give considerable flexibility to the design and placement of indicators, it is recommended that Power and LAN Status indicators follow the recommendations in the LXI Specifications.

# **RECOMMENDATION 3.3:** AXIe-0 modules and chassis SHOULD follow the Recommendations for Indicator Color, State, and Labeling as described in the LXI Specification Section 2.5 Electrical Standards – Status Indicators.

# **RECOMMENDATION 3.4:** Place indicators near the top of a faceplate when the module is oriented vertically for the highest visibility.

#### 3.2.2.2 Device Label Requirements

AXIe-0 products do not require an LXI logo as are required for LXI devices. This is due to AXIe-0 devices taking exceptions to some portions of the LXI Specification and the small surface area for placing a label. However, like LXI, an AXIe-0 module must include its MAC address somewhere on the module.

PERMISSION 3.4: An AXIe-0 device MAY be designed without an LXI label.

RULE 3.8: An AXIe-0 module that utilizes LAN SHALL label its MAC address somewhere on the module.

**OBSERVATION 3.4:** The MAC address label may be placed on the faceplate or on a module shield

**RECOMMENDATION 3.5:** Locate the MAC address label on the faceplate if space is available.

**OBSERVATION 3.5:** Labels on the module shield may only be readable when the module or adjacent modules are removed. Labels on the faceplate are viewable when all modules are inserted into the chassis.

#### 3.2.2.3 Device Button Requirements

RULE 3.9: An AXIe-0 device that utilizes LAN SHALL provide a LAN Reset mechanism available from the faceplate of an inserted module.

**RECOMMENDATION 3.6:** Locate the LAN reset button behind a small hole on the faceplate that is accessible only with an inserted tool.

**OBSERVATION 3.6:** The LAN reset function is identical to the LCI (LAN Configuration Initialize) function of LXI, resetting the device to this configuration found in Section 8.13 of the LXI Specification:

#### Table of items affected by LAN Configuration Initialize Mechanism

| Item                           | Value                       | Section                    |
|--------------------------------|-----------------------------|----------------------------|
| IP Address Configuration:      |                             |                            |
|                                |                             | 8.6                        |
| • DHCP                         | <ul> <li>Enabled</li> </ul> |                            |
| • AutoIP                       | <ul> <li>Enabled</li> </ul> |                            |
| ICMP Ping Responder            | Enabled                     | 8.3                        |
| Web Password for configuration | Factory Default             | 9.8                        |
| Dynamic DNS (if implemented)   | Enabled                     | 8.11.1.1                   |
| mDNS and DNS-SD                | Enabled                     | 10.3, 10.4, 10.5.1, 10.7.1 |

#### Table 3-1. Items affected by LAN Configuration Initialize Mechanism

In the above table, the Section column refers to sections in the LXI Specification.

#### 3.2.3 LAN/LXI Synchronization and Events

LXI specifies several methods pertaining to synchronization and events. AXIe-0 adds no additional requirements. IEEE 1588 operation and events are optional.

**RULE 3.10:** IF an AXIe-0 device utilizes LXI Event Messaging, LXI Clock Synchronization, or LXI Event Logging, THEN it SHALL implement those functions in accordance with LXI Specification Section 3 LXI Device Synchronization and Events.

PERMISSION 3.5: An AXIe-0 module MAY enable IEEE 1588 synchronization from its LAN connection.

**RULE 3.11:** IF an AXIe-0 device utilizes IEEE 1588, THEN it SHALL follow the IEEE 1588 Rules documented in the LXI Specifications.

PERMISSION 3.6: An AXIe-0 chassis instrument MAY drive AXIe TRIG lines derived from IEEE 1588 operation.

**OBSERVATION 3.7:** The **PERMISSION** above allows a single **IEEE 1588** device in a chassis to deliver synchronization events to all modules in an AXIe-0 chassis.

#### 3.2.4 LAN/LXI Module-to-Module Data Communication of LXI Event Messages

This section describes the data format for direct module-to-module messages. AXIe-0 adds no requirements over that of the LXI Specification. The rules and content for these functions has been moved to the LXI Event Messaging Extended Function.

#### 3.2.5 LAN/LXI Device Wired Trigger Bus

The LXI Wired Trigger Bus does not exist in AXIe-0, but the AXIe TRIG bus is a very effective substitute, as it connects all devices in a chassis to the same trigger bus. An LXI chassis or system module may implement the LXI Wired Trigger Bus to connect to another AXIe-0 chassis or external LXI device.

#### 3.2.6 LAN/LXI Programmatic Interface (Drivers)

AXIe-0 devices communication using LAN. The specific protocol is not specified, but a driver is required compliant with driver specifications in the IVI Foundation at <u>https://www.ivifoundation.org</u>. IVI is an abbreviation for Interchangeable Virtual Instruments. Also found at the IVI Foundation are the specifications for SCPI, Standard Commands for Programmable Instruments. SCPI may, or may not, be deployed on any specific device. LXI presumes the primary control interface is IVI.

#### RULE 3.12: AXIe-0 devices with LAN access SHALL provide one or more IVI drivers.

**RECOMMENDATION 3.7: IF an AXIe-0 device delivers an IVI driver THEN it SHOULD deliver an IVI-C driver.** 

**OBSERVATION 3.8:** The protocol between a driver and the device is vendor-specific.

PERMISSION 3.7: An AXIe-0 device MAY use non-SCPI commands.

PERMISSION 3.8: An AXIe-0 MAY use SCPI commands.

RULE 3.13: An AXIe-0 device with LAN SHALL implement Device Identity indicator.

**OBSERVATION 3.9:** The Device Identity indicator uses the LAN Status indicator(s).

RULE 3.14: An AXIe-0 device that detects slot location SHALL report slot location via its IVI driver.

**RULE 3.15:** IF an AXIe-0 device delivers functionality described in LXI Specifications Section 6 LXI Programmatic Interfaces (Drivers) THEN it SHALL comply to all relevant RULES in that section.

#### 3.2.7 LAN Specifications

AXIe-0 devices generally follow the rules documents in the LXI Specification Section 7 LAN Specifications. The labels requirement previously specified that the MAC address be displayed on the faceplate or should of a module. The LAN switch in the system module operates at GbE, while the modules must support 100Mbits/sec, but may also support GbE or 10Mbits/sec.

RULE 3.16: An AXIe-0 system module, whether explicit or embedded, SHALL implement Auto-MDIX.

**PERMISSION 3.9:** An AXIe-0 module MAY be designed to not implement Auto-MDIX.

**OBSERVATION 3.10:** Chassis Auto-MDIX is sufficient for all modules.

RULE 3.17: An AXIe-0 system module, whether explicit or embedded, SHALL support GbE.

RULE 3.18: An AXIe-0 device SHALL operate in Ethernet networks at 100Mbits/sec.

PERMISSION 3.10: An AXIe-0 module MAY operate at GbE.

PERMISSION 3.11: An AXIe-0 module MAY operate at 10Mbits/sec.

RULE 3.19: An AXIe-0 device SHALL implement Ethernet Connection Monitoring.

#### 3.2.8 IPV4 LAN Configuration

AXIe-0 devices generally follow the rules documents in the LXI Specification Section 8 IPv4 LAN Configuration.

RULE 3.20: An AXIe-0 device SHALL implement IPv4.

RULE 3.21: An AXIe-0 device SHALL comply with Section 8 of the LXI Specification.

PERMISSION 3.12: An AXIe-0 device MAY implement IPv6.

RULE 3.22: An AXIe-0 device SHALL support ICMP Ping Responder.

**RULE 3.23:** An AXIe-0 device SHALL support LXI IP address configuration techniques as shown in the following figure.

|   | Automatic IP<br>Configuration Methods  |   | Manual IP Configuration<br>Methods |
|---|--|---|------------------------------------|
| Network Topology  | DHCP   | Dynamic Link-Local<br>Addressing  | Manual IP Address<br>Configuration |
| Instrument as<br>Shared<br>Resource                             | Works on nearly all<br>site/enterprise LANs<br>because they are built<br>with DHCP               | STOP<br>Auto-IP not likely to be<br>used here                           | Works in all<br>network topologies |
| Router Computer<br>Private LAN<br>Test System                   | Works on network built<br>with Ethernet router with<br>integrated DHCP server<br>(or equivalent) | STOP<br>Auto-IP not likely to be<br>used here                           | Works in all<br>network topologies |
| Computer<br>Private LAN<br>II Instrument<br>Multi-instr Desktop | Works on network built<br>with Ethernet router with<br>integrated DHCP server<br>(or equivalent) | Works on network built<br>with Ethernet switch/hub<br>(i.e. w/o DHCP)   | Works in all<br>network topologies |
| Computer<br>Desktop<br>Crossover Cable<br>Instrument            | DHCP not likely to be<br>used here   | Works on 2-node<br>network built with a<br>crossover cable (no<br>DHCP) | Works in all<br>network topologies |

#### Applicability of Configuration Methods to Network Topologies

Figure 3-2: LAN Configuration Methods

RULE 3.24: An AXIe-0 device SHALL support one of the following options for LAN configuration:

- A single configuration setting of Automatic (implying DHCP and Dynamically Configured Link Local Addressing) or Manual.
- Individual configuration settings for: DHCP, Dynamically Configured Link Local Addressing, and Manual.

RULE 3.25: IF more than one configuration method is included, THEN the LXI Device's LAN configuration SHALL proceed in the following order: 1) DHCP, 2) Dynamically Configured Link Local Addressing, 3) manual.

**RECOMMENDATION 3.8:** AN AXIe-0 device SHOULD use Dynamic DNS capabilities as outlined in the LXI Specification.

#### 3.2.9 Web Interface

AXIe-0 devices generally follow the rules documents in the LXI Specification Section 9 Web Interface.

#### RULE 3.26: An AXIe-0 device SHALL comply with LXI Specification Section 9 Web Interface.

**RULE 3.27:** An AXIe-0 device SHALL display an LXI welcome page with the following information in a readonly format:

- LXI Device Model
- Manufacturer
- Serial Number
- Description
- LXI Extended Functions
- LXI version
- Hostname
- MAC Address <XX-XX-XX-XX-XX>
- TCP/IP Address <DDD.DDD.DDD.DDD>
- Firmware and/or Software Revision
- LXI Device Address String [VISA]

**RULE 3.28:** An AXIe-0 device SHALL display an LXI configuration page containing the following parameters:

- Hostname
- Description
- TCP/IP Configuration Mode
- Static IP address
- Subnet mask
- Default Gateway
- DNS Server(s)

An example of an LXI configuration page is shown below:

| e Edit View Fevorites Tools Help                  | 2133 - Herristen Distantes California |                          | THE COLUMN                         |
|---|---------------------------------------|--------------------------|------------------------------------|
| Back - + - ) : () () Search @Fa                   | vartes Meda 3 3. 9 10 .               |                          |                                    |
| //  |                                       |                          | Example Test Inc                   |
| Home  | Advanced IP Configu                   | iration                  |                                    |
| Synchronization Configuration                     | Link speed                            | Auto                     |                                    |
| Status<br>Security                                | TOMP Ping                             | O Disabled               |                                    |
| Instrument Configuration                          | mDNS Discovery                        | O Disabled               |                                    |
| Datasheet<br>Manual                               | Dynamic DNS updates                   | O Disabled<br>() Enabled |                                    |
| Driver Download<br>Help                           | VXI-11 Discovery                      | O Disabled<br>Enabled    |                                    |
| For help and support, please visit<br>our website | Submit. Reset.                        |                          |                                    |
|   | - Simple IP Configuration             |                          |                                    |
| 111   |                                       |                          | Lan eXtensions for Instrumentation |

Figure 3-3: Example LAN Configuration Page

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### 3.2.10 LAN Discovery and Identification

AXIe-0 devices generally follow the rules documents in the LXI Specification Section 10 LAN Discovery and Identification.

RULE 3.29: An AXIe-0 device SHALL comply with LXI Specification Section 10 LAN Discovery and Identification.

RULE 3.30: An AXIe-0 device SHALL support mDNS discovery protocol from LXI.

PERMISSION 3.13: An AXIe-0 device MAY support VXI-11.

### 3.3 LXI Extended Functions

LXI describes Extended Functions which can be found here:

AXIe-0 devices, if they include an extended function, generally follow the rules documented in the appropriate extended function.

#### 3.3.1 LXI Event Log Extended Function

PERMISSION 3.14: An AXIe-0 device MAY support LXI Event Log Extended Function.

3.3.2 LXI VXI-11 Discovery and Identification Extended Function PERMISSION 3.15: An AXIe-0 device MAY support VXI-11 Discovery and Identification Extended Function.

3.3.3 LXI Timestamped Data Extended Function PERMISSION 3.16: An AXIe-0 device MAY support LXI Timestamped Data Extended Function.

3.3.4 LXI HiSLIP Extended Function v1\_02 PERMISSION 3.17: An AXIe-0 device MAY support LXI HiSLIP Extended Function.

3.3.5 LXI Clock Synchronization Extended Function PERMISSION 3.18: An AXIe-0 device MAY support LXI Clock Synchronization Extended Function.

#### 3.3.6 LXI Event Messaging Extended Function

PERMISSION 3.19: An AXIe-0 device MAY support LXI Event Messaging Extended Function.

### 3.3.7 LXI Wired Trigger Bus Extended Function

The LXI Wired Trigger Bus is a hardwired interface that interconnects multiple LXI devices. Hardware triggering offers trigger accuracy in the nanosecond range. This compares favorably to software triggering via LAN, which is typically in the millisecond range. Since AXIe-0 offers an embedded trigger bus, most hardwired trigger operations would occur within an AXIe-0 chassis. However, there may be a situation when an AXIe-0 chassis would be integrated with other LXI instruments in a measurement system and synchronized using the LXI Wired Trigger Bus between the AXIe-0 chassis and a discrete LXI device. The AXIe-0 chassis would map the trigger lines to the trigger lines on the AXIe-0 backplane.

#### PERMISSION 3.20: An AXIe-0 chassis MAY support LXI Wired Trigger Extended Function.

#### 3.3.8 LXI IPv6 Version v1\_1

PERMISSION 3.21: An AXIe-0 device MAY support LXI IPv6 Version v1\_1.

# 4. Documentation

Documentation is required to design an AXIe-0 system and choose the various system components. For example, to decide whether a system consisting of an AXIe-0 chassis and one or more AXIe-0 modules is compatible, it is necessary to ensure that the per slot power and cooling requirements of all modules can be met with the per-slot and total power and cooling capacity of the chassis. This section details the documentation required for any AXIe-0 module or chassis.

# 4.1 Required Documentation of AXIe-0 chassis

RULE 4.1: An AXIe-0 chassis SHALL document the capabilities outlined in Table 4-1.

| AXIe-0 Chassis Documentation Requirements |   |
|---|---|
| Capability                                | Notes   |
| Number of slots                           |   |
| Embedded or AXIe System Module            | States whether a slot for the System Module, or if it is Embedded |
| Power Capability per Slot                 |   |
| Total Power Capability                    |   |
| Cooling Capability per Slot               |   |
| Total Cooling Capability                  |   |
| Local Bus Capability                      | States whether local bus is offered                               |

Table 4-1. Required capability documentation for an AXIe-0 chassis

## 4.2 Required Documentation of AXIe-0 modules

RULE 4.2: An AXIe-0 chassis SHALL document the capabilities outlined in Table 4-1.

| AXIe-0 Module Documentation Requirements |                                      |  |
|--|--------------------------------------|--|
| Capability                               | Notes                                |  |
| Number of slots                          |                                      |  |
| Maximum Power Required for Any Slot      |                                      |  |
| Total Power Required                     |                                      |  |
| Maximum Cooling Required for Any Slot    |                                      |  |
| Total Cooling Required                   |                                      |  |
| Local Bus Requirement                    | States whether local bus is accessed |  |

#### Table 4-2. Required capability documentation for an AXIe-0 module